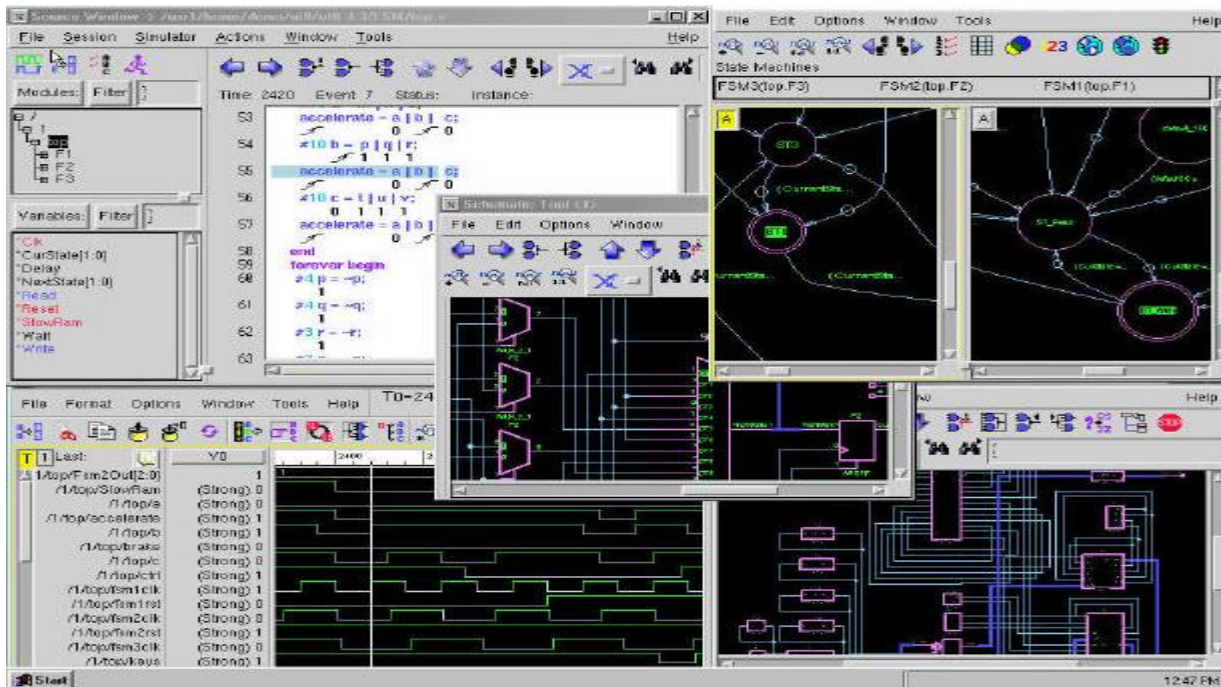


VeritoolsDesigner-Universal

Veritools LINUX Source Code Debugging suite for Verilog/VHDL/SystemVerilog now runs native on Windows.



A complete suite of tools for source code debugging and SystemVerilogAssertion verification, is now ported to the Windows PC

Source Code Debugging

- Runs native on Windows and on Linux
- Source Code debugging for Verilog, VHDL, and SystemVerilog, and SystemVerilog Assertions
- RTL and Gate Schematic Window
- State Diagram Window
- PLI and VHPLI waveform data file compression over 1,000 X, much faster simulation speeds
- Control Flow Graph Window

SVAssertion based Verification

- Speeds up Verification process 10-100 X
- Standalone SystemVerilog Assertion Simulator with SVA Analyzer
- Easy to use, graphical SVA debugging
- “What if” window for rapid testing of new SystemVerilog assertions
- Re-run new assertions using simulation results file (no re-simulation required)
- Eliminate simulation slowdown due to SVA evaluation

Download VeritoolsVerify from our web site: www.veritools.com

330 Lunada Drive, Los Altos, CA 94022; phone: (650) 949-8665 cell: (650) 533-5595; e-mail: inquiry@veritools.com

The only reasonably priced, advanced Source code debugger currently on the market

Source Code Debugging

VeritoolsDesigner provides a completely integrated RTL/Gate source code debugging suite for the design and debugging of Verilog, VHDL and SystemVerilog and SystemVerilog Assertions.

Waveform Display: Provides instant display of waveform files that are many gigabytes in size. New technology allows almost instant viewing of users' waveform data files even for these huge files. Signal data can be analog or digital or mixed analog/digital data and can be in any of the many formats Veritools supports. The Undertow waveform viewer can display almost instantly, optimized compressed files that are compressed by a factor over 1,000X.

Source Code Display: This window provides information on signal drivers, and/or loads and are synchronized in time to the waveform window. Users can trace back any signal through an unlimited number of modules or files to find why the signal has transitioned. This window will now allow automatic trace back of any signal value through any number of levels, including FFs. These windows can identify the exact line of code that causes any X or any signal edge to transition with a single cursor snap in the waveform window.

Schematic Display, RTL or Gates: These windows display the RTL or gate schematic for any signal or any element from any other window. Users can automatically trace back any signal or element to see the drivers to any level or to trace forward any element or signal to any level. Signal values are annotated right onto the schematic window to allow for rapid trace back/forward of any signal.

Control Flow Graph Users can automatically trace signal values back through any number of FFs to the error condition that caused this signal to go to this value in the first place. This feature combines "Trace Input Cone", the feature that allows users to automatically trace signal values back to a primary FF, with time lines on the schematic window to display the points in time where this signal value passed through FF elements.

State Diagram Display: Automatically extract virtually every type of state diagram from the users' source code. Users can display any number of state diagrams at the same time, step their state diagrams forward or backward, and use the state diagram analysis tools to determine state coverage, state coincidence and states that cannot be reached or which have no exit.

Perl Scripts: Built-in Perl scripting analysis tools provide a huge increase in productivity. The Perl scripts can be run with the Undertow GUI up or in a batch process.

File Compression over 1,000 X: When running any of the digital simulators, the Veritools' PLI/VHDLPLI can be used in order to get a highly compressed file output, over 1,000 X times smaller than VCD files.

Speed and features not available in other tools at any price.

SystemVerilog Assertion Based Verification

VeritoolsVerifier provides for a higher level of design verification allowing a significantly higher percentage of first silicon success with a powerful stand-alone evaluator for SystemVerilog Assertions. The analysis of assertions can be done using

the users' current simulation result files. Since SystemVerilog has a concept called "bind", users can bind-in SV Assertions to their existing or new Verilog or VHDL designs and continue to do simulation with their current simulators with no change to their current design process. Embedded SV Assertions using a SystemVerilog simulator is also supported.

SV Assertion control and evaluation

The VeritoolsVerifier can display exactly where all of the user's design SV Assertions are located in the design hierarchy and can evaluate each assertion for "pass", "fail" or "vacuously true". The assertion evaluation results are then displayed in a color-coded design hierarchy. Since simulation result files are used for the analysis of the SV Assertions, it is possible to do the analysis on the users SV Assertions an unlimited number of times in a pure batch process without the requirement for doing any additional re-simulation cycles.

Graphical Waveform Display of Assertion Results

Assertion results can be displayed in a graphical waveform window along with the timing for each assertion and the components and local variables that are part of each assertion. Since it is possible that each assertion can be triggered at each and every clock cycle, a signal "Go To" icon allows users to go exactly to the point where each assertion has gone active and has either passed or failed the evaluation. Users can then use these time points in order to display the assertion timing and assertion components for this selected assertion evaluation.

"What-if" Window

The assertion "What if" window allows users to create, modify and disassemble SV Assertions, and then quickly re-evaluate these assertions an unlimited number of times without requiring the users to re-simulating their design. Each new SVA evaluations can be done very quickly even when using enormous result files.

Simulation Speed

When SV Assertions are part of the design simulation process, users often experience severe degradation of simulator speed. Since the SV Assertion analysis can now be completely removed and done outside of the design simulation step, the severe degradation of simulator speed caused by SVA evaluations can be completely eliminated. The combination of the "what If window and the faster visualization times means that the process of creating and evaluating SV Assertions can be significantly faster and at much less cost than using a "simulator only" approach. Users, whose designs in many cases are approaching 100,000 lines of assertion code, can debug both their assertions and their design in a fraction of the time previously required with a "simulator only" approach.

Veritools Verifier/Designer/vWave

The most advanced **Source Code Debugging** and **Waveform Viewing** tools on the market, all are part of the same binary.

- Provides **analog and digital waveform viewing, automatic state diagram and RTL/Gate schematic extraction** and viewing,
- Also provides a **SystemVerilogAssertion simulator and analyzer** so user can debug their SV Assertions, a “**what if window**” allows **instant verification** of assertion modifications.
- Provides the **most advanced Verilog 2012 pre-compiling, parsing, elaboration and source code linting** on the market.
- Provides **ability to convert users Verilog 2012 to Verilog 2005**, so users can write Verilog 2012, and use Verilog 2005 tools
- These tools have a **GUI configuration window** so users can **configure their GUI to any configuration they like in minutes**.

The **only advanced source code debugging software** that is **reasonably priced**.

Why pay for outrageously overpriced software with exactly the same yet fewer functions with even **the exact same GUI?**

