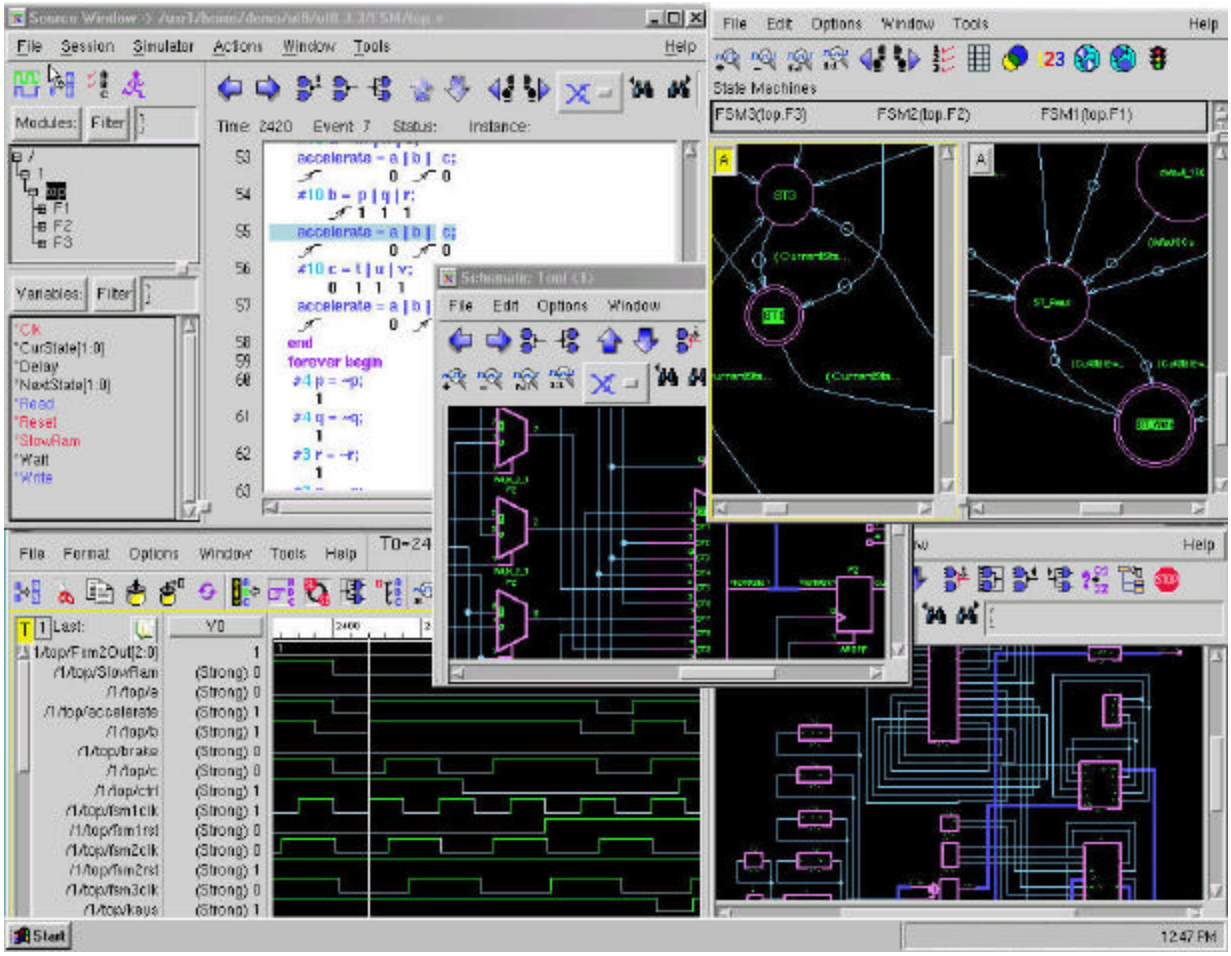
VeritoolsDesigner

Debugging tool suite for Verilog, VHDL, and SystemVerilog RTL and Gate Designs



A complete suite of tools to do SystemVerilog Assertion based verification and source code design and debugging

Source Code Debugging

- Load/display very large files (20 gig+) in seconds
- Source Code debugging for Verilog, VHDL, and SystemVerilog
- RTL and Gate Schematic Views
- State Diagram Views
- PLI and VHPLI waveform data file compression of 1,000 X faster simulation
- Control Flow Graph

SVAssertion based Verification

- Increase rate of 1st Silicon Success
- Standalone SystemVerilog Assertion Analyzer with built-in SVA compiler
- Easy to use, graphical SVA debugging
- "What if" window for rapid testing of new SystemVerilog assertions
- Re-run new assertions using simulation results file (no re-simulation required)
- Eliminate simulation degradation due to SVA evaluations

Veritools

Download VeritoolsVerify from our web site: www.veritools.com

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Design, debug, and verify your design in a fraction of the time!

Source Code Debugging

VeritoolsDesigner provides a completely integrated environment for the design and debugging of Verilog, VHDL and SystemVerilog allowing an unlimited number of time-synchronized windows.

Waveform Display: Provides instant display of waveform files that are many gigabytes in size. New technology allows almost instant viewing of users' waveform data files even for these huge files. Signal data can be analog or digital or mixed analog/digital data and can be in any of the many formats Veritools supports. The Undertow waveform viewer can read almost instantly, even the optimized compressed files that are compressed by a factor over 1,000X.

Source Code Display: These windows provide information on signal drivers, and/or loads and are synchronized in time to the waveform window. Users can trace back any signal through an unlimited number of modules or files to find why the signal has transitioned. This window will now allow automatic trace back of any signal value through any number of levels, including FFs. These windows can identify the exact line of code that causes any signal edge to transition with a single cursor snap in the waveform window.

Schematic Display, RTL or Gates: These windows display the RTL or gate schematic for any signal or any element from any other window. Users can automatically trace back any signal or element to see the drivers to any level or to trace forward any element or signal to any level. Signal values are annotated right onto the schematic window to allow for rapid trace back/forward of any signal.

Control Flow Graph Users can automatically trace signal values back through any number of FFs to the error condition that caused this signal to go to this value in the first place. This feature combines "Trace Input Cone", the feature that allows users to automatically trace signal values back to a primary FF, with a time line on a schematic window to display the points in time where this signal value passed through FF elements.

State Diagram Display: Automatically extract virtually every type of state diagram from the users' source code. Users can display any number of state diagrams at the same time, step their state diagrams forward or backward, and use the state diagram analysis tools to determine state coverage, state coincidence and states that can not be reached or which have no exit.

Perl Scripts: Built-in Perl scripting analysis tools provide a huge increase in productivity. The Perl scripts can be run with the Undertow GUI up or in a batch process.

File Compression over 1,000 X: When running any of the digital simulators, the Veritools' PLI/VHDLPLI can be used in order to get a highly compressed file output, over 1,000 X times smaller than a VCD file.

SystemVerilog Assertion Based Verification

VeritoolsVerifier provide for a higher level of design verification allowing a significantly higher percentage of first silicon success with a powerful stand alone evaluator for SystemVerilog Assertions. The analysis of assertions can be done using the users' current simulation result files. Since SystemVerilog has a concept called "bind", users can bind-in SVAssertions to their existing or new Verilog or VHDL designs, and continue to do simulation with their current simulators with no change to their current design process. Embedded SVAssertions using a SystemVerilog simulator is also supported.

SVAssertion control and evaluation

The VeritoolsVerifier can display exactly where all of the users design SVAssertions are located in the design hierarchy and can evaluate each assertion for "pass", "fail" or "vacuously true". The assertion evaluation results are then displayed in a color-coded design hierarchy. Since simulation result files are used for the analysis of the SVAssertions, it is possible to do the analysis on the users SVAssertions an unlimited number of times in a pure batch process without the requirement for doing any additional re-simulation cycles.

Graphical Waveform Display of Assertion Results

Assertion results can be displayed in a graphical waveform window along with the timing for each assertion and the components and local variables that are part of each assertion. Since it is possible that each assertion can be triggered at each and every clock cycle, a signal "Go To" icon allows users to go exactly to the point where each assertion has gone active and has either passed or failed the evaluation. Users can then use these time points in order to display the assertion timing and assertion components for this selected assertion evaluation.

"What-if" Window

The assertion "What if" window allows users to create, modify and disassemble SVAssertions, and then quickly re-evaluate these assertions an unlimited number of times without requiring the uses to re-simulating their design. Each new SVA evaluations can be done very quickly even when using enormous result files.

Simulation Speed

When SVAssertions are part of the design simulation process, users often experience severe degradation of simulator speed. Since the SVAssertion analysis can now be completely removed and done outside of the design simulation step, the severe degradation of simulator speed caused by SVA evaluations can be completely eliminated. The combination of the "what If window and the faster visualization times means that the process of creating and evaluating SVAssertions can be significantly faster and at much less cost than using a "simulator only" approach. Users, whose designs in many cases are approaching 100,000 lines of assertion code, can debug both their assertions and their design in a fraction of the time previously required with a "simulator only" approach.

The speed and features not available in other tools at any price.

All of the features of Undertow Suite are available in both interactive mode, or in batch mode for use in virtual simulation, without using a simulator license. VeritoolsVerify supports **Verilog, Verilog 2001, VHDL, SystemC** and **SystemVerilog**, and SystemVerilog Assertion analysis including tools for assertion metrics to allow coverage analysis. Veritools products are available on 32- and 64-bit Sun _Solaris, HP700/800, IBM AIX, in addition to Windows 98/NT/2000/XP and Linux systems.